Change 1

In the electrical spec table for the line called OCP hiccup time with typical value of 40ms please add the following in the 'test conditions/comments' column: "See INPUT/OUTPUT CURRENT LIMIT PROTECTION section"

Change 2

In the INPUT/OUTPUT CURRENT LIMIT PROTECTION section please add the following text after the paragraph that ends with "…enters the 45 ms hiccup mode"

"Under certain situations the ADP1074 will exit OCP hiccup mode. In this condition, even though the COMP pin will be at the maximum clamp level, the device will not enter hiccup mode. It is guaranteed that the PWMs will be terminated whenever the CS maximum threshold is reached. The conditions under which this can occur are:

Under certain conditions, the ADP1074 OCP hiccup mode. In these conditions, the COMP pin is at the maximum clamp level, but the device does not enter hiccup mode. However, it is guaranteed that the PWMs are terminated whenever the CS maximum threshold is reached. The condition under which ADP1074 skips entering hiccup mode is when VDD2 is powered through an auxiliary winding and an output short circuit occurs that results in the FB pin having a voltage that is less than 300 mV. This event is more prominent at high temperatures (>85°C), and can be exacerbated at higher temperatures.

The root cause of the device exiting hiccup mode is due to the effect that the OCP hiccup mode feature has on the SS2 pin. During OCP recovery, the SS2 pin tracks the FB pin and attempts a soft start from the precharge sequence. During this time that SS2 tracks FB, the SS2 pin can be less than the FB pin for a short interval, which causes the COMP pin (output of the gm amplifier) to momentarily dip below the maximum COMP pin clamp level. This event means that the current limit required for the next few switching periods is less than the maximum threshold and puts the device out of hiccup mode, because the ADP1074 fails to register 1.25ms worth of consecutive over current cycles and fails to enter OCP hiccup mode.

To guarantee OCP hiccup mode, the following circuits is recommended, based on the configuration of the VDD2 power supply:

1. When VDD2 is powered directly from the output voltage, if a short circuit on the output terminals of the load occurs after steady state regulation is achieved, the VDD2 pin is less than the UVLO, and the device enters hiccup mode for 200 ms, similar to the hiccup time described in the **Error! Reference source not found.** section.
2. When VDD2 is powered through auxiliary winding or another configuration, when a short circuit occurs on the output terminals, the auxiliary winding is not shorted and maintains a positive voltage above the VDD2 UVLO threshold. To enter hiccup mode, the following circuit is recommended, as shown in Figure 15. The circuit operates as follows: when the output voltage goes low due to a short circuit, the D1 diode turns on, which pulls the base of the BJT { Bipolar Junction Transistor} low, shutting off VDD2. The system then enters hiccup mode, as described in the **Error! Reference source not found.** section.

   R3 is sized to bias the Zener diode and R4 is sized such that $(V_{ZENER} - 1)/R4 > I_{ZENER}$, where V_{ZENER} is the voltage of the diode and I_{ZENER} is the biasing current of the diode. This sizing ensures that the impedance of the resistor is less than the impedance of the diode, which causes the voltage of the diode to drop, and allows VDD2 to enter UVLO.

   If the output voltage is <5 V, the same procedure can be used to size the R4 resistor. If a discrete LDO is not used, a simple resistor and diode connector to the output voltage is sufficient. In this case, the R4 resistor is

sized to limit the current through the D1 diode when the output voltage is 0 V during a short circuit event. Because the bandwidth of the system is high, the ADP1074 is able to maintain voltage regulation at the proper voltage level, even if the auxiliary winding voltage is higher than the output voltage. The soft start and soft start from precharge conditions is met with the addition of this circuit due to the bandwidth of the overall system.

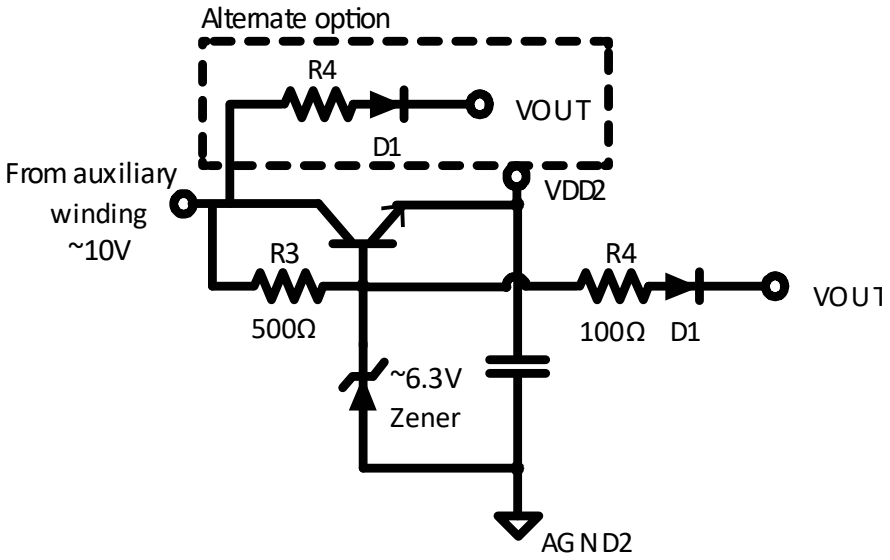

Figure 15. Recommended circuit to Guarantee Hiccup Mode Showing Typical Values